**Lesson Plan –ANALOGNAND DIGITAL ELECTRONICS (CS301ES)**

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| Faculty Name:SHYAM K | Year / Sem: II/I | Academic Year: 2021-22 |

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| **SL. No** | **Name of the Topic** | | | **Plan Date** | **Actual Date** | **Remarks** |
| 1 | **Unit 1: Diodes and Aplications,** Introduction to subject | | | 18/10/21 | 25/10/21 |  |
| 2 | Junction diode characterstics,open circuit PN junction | | | 21/10/21 | 26/10/21 |  |
| 3 | PN junction as rectifier,VI characterstics | | | 22/10/21 | 28/10/21 |  |
| 4 | Effect of temperature,diode resistance | | | 25/10/21 |  |  |
| 5 | Diffusion capacitance,diode swiching times | | | 26/10/21 |  |  |
| **T1** | Diodes and Aplications, Introduction to subject | | | 28/10/21 |  |  |
| 6 | Breakdown diodes,Tunnel ,diodes,photo diodes | | | 29/10/21 |  |  |
| 7 | LED,diode aplications-clipping circuits | | | 1/11/21 |  |  |
| 8 | Comparators | | | 2/11/21 |  |  |
| **T2** |  | | | 5/11/21 |  |  |
| 9 | Half wave rectifier | | | 8/11/21 |  |  |
| 10 | Full wave rectifier | | | 9/11/21 |  |  |
| 11 | Rectifier with capacitor | | | 11/11/21 |  |  |
| 12 | Basic theorems | | | 12/11/21 |  |  |
| **T3** | comparators | | | 15/11/21 |  |  |
| **T4** | Half wave rectifier | | | 16/11/21 |  |  |
| 12 | **Unit-II: BJTs Transistor characteristics** | | | 18/11/21 |  |  |
| 13 | The junction transistor | | | 19/11/21 |  |  |
| 14 | Transistor as an amplifier | | | 22/11/21 |  |  |
| 15 | CB &CE configurations | | | 23/11/21 |  |  |
| **T5** | Half wave rectifier | | | 25/11/21 |  |  |
| 16 | CC configuration,comparision of transistor configurations | | | 26/11/21 |  |  |
| 17 | The operating point,self bias or emitter bias, | | | 29/11/21 |  |  |
| 3018 | Bias compensation,thermal runaway and stability | | | 29/11/21 |  |  |
| 19 | Transistor at low frequencies | | | 30/11/21 |  |  |
| **T6** | Thermal runaway and stability | | | 30/11/21 |  |  |
| 20 | CE amplifier response,Gain band width product | | | 2/12/21 |  |  |
| 21 | Emitter follower | | | 2/12/21 |  |  |
| 22 | RC coupled amplifier | | | 3/12/21 |  |  |
| 27 | Two cascaded CE amplifier | | | 3/12/21 |  |  |
| **T7** | Emitter follower | | | 3/12/21 |  |  |
| 28 | Multistage CE amplifiers | | | 6/12/21 |  |  |
| 30 | **Topic beyond the syllabus** | | | 6/12/21 |  |  |
| 31 | **Topic beyond the syllabus** | | | 7/12/21 |  |  |
| **T8** | Multistage CE amplifiers | | | **7**/12/21 |  |  |
|  | | Slip Test:9/12/21 | | | | |
| 32 | **Unit-III: FETs and Digital Circuits** FETs | | | 10/12/21 |  |  |
| 33 | JFET,VI Characterstics,MOSFET | | | 10/12/21 |  |  |
|  | | **Assignment-I Issue date:**9/12/21 **Submission date:**11/12/21 | | | | |
|  | **I Mid Examination** | | | 13/12/21 |  | |
| 34 | Low frequency CS and CD amplifiers | | | 20/12/21 |  |  |
| 35 | CS and CD amplifiers | | | 21/12/21 |  |  |
| **T9** | FETs | | | 21/12/21 |  |  |
| 36 | Digital circuits:digital binary operations of a system | | | 23/12/21 |  |  |
| 37 | OR gate,AND gate,NOT gate | | | 24/12/21 |  |  |
| 38 | EXOR-gate | | | 2/12/21 |  |  |
| 39 | Demorgan laws | | | 28/12/21 |  |  |
| **T10** | EXOR-gate | | | 28/12/21 |  |  |
| 40 | NAND AND NOR DTL gates | | | 28/12/21 |  |  |
| 41 | Modified DTL gates | | | 30/12/21 |  |  |
| 42 | HTL and TTL gates | | | 31/12/21 |  |  |
| 43 | Output stages,RTL and DCTL | | | 3/01/22 |  |  |
| **T11** | Modified DTL gates | | | 4/01/22 |  |  |
| 44 | CMOS | | | 4/01/22 |  |  |
| 45 | Comparison of logic families | | | 6/01/22 |  |  |
| **T12** | CMOS | | | **7**/01/22 |  |  |
| **Slip Test:** 10/01/22 | | | | | | |
| 48 | **(Gap identified beyond the syllabus)** | | | 7/01/22 |  |  |
| 49 | **(Gap identified beyond the syllabus)** | | | 7/01/22 |  |  |
| 50 | **Unit IV: Combinational Logic Circuits**  Basic theorems and properties of Boolean algebra | | | 11/01/22 |  |  |
| 51 | Canonical and standard forms | | | 13/01/22 |  |  |
| 52 | Digital logic gates | | | 14/01/22 |  |  |
| 53 | The map method | | | 14/01/22 |  |  |
| **T13** | **Explanation of state diagram with one example** | | | 14/01/22 |  |  |
| **54** | Product of sums simplifications | | | 17/01/22 |  |  |
| 55 | Don’t care conditions, NAND and NOR implementation | | | 18/01/22 |  |  |
| 56 | Exclusive-OR function | | | 20/01/22 |  |  |
| 57 | Binary adder-subtractor | | | 21/01/22 |  |  |
| **T14** | **Design FSM which Detect the sequence 1111 by using JK flip flop** | | | 21/01/22 |  |  |
| 58 | Decimal adder, binary multiplier | | | 24/01/22 |  |  |
| 59 | Magnitude comparator,decoders | | | 25/01/22 |  |  |
| 60 | Encoders,multiplexers | | | 25/01/22 |  |  |
|  | | **Slip Test:27/01/22** | | | | |
| 61 | **Unit V: Sequential logic circuits:** sequential circuits | | | 28/01/22 |  |  |
| **T15** |  | | | 28/01/22 |  |  |
| 62 | Storage elements | | | 31/02/22 |  |  |
| 63 | Lacthes and flipflops | | | 1/02/22 |  |  |
| 64 | Analysis of clocked sequencial circuits | | | 3/02/22 |  |  |
| 65 | State reduction and assignment,shift registers | | | 4/02/22 |  |  |
| 66 | Ripple counters,synchronous counter | | | 7/02/22 |  |  |
| 67 | RAM AND ROM | | | 8/02/22 |  |  |
| **T16** | **Limitations and Capabilities of FSM and problem solving on partition method and merger method** | | | 10/02/22 |  |  |
| 68 | Revision | | | 10/02/22 |  |  |
|  | | **Slip Test:**11/02/22 | | | | |
|  |  | | **Assignment-II Issue date** 10/02/22 **Submission date:** 12/02/22 | | | |
|  | **Mid-2 Examination** | | | **14/02/22** |  | |

**TEXT BOOKS**:

T1**:**Integrated electronics Analog and digital circuits and systems,2/e,Jacob millman.

T2:Digital design,5/e,Morris Mano and Michel

**REFERENCE BOOKS:**

R1**:** Electronics Devices and Circuits ,Jimmy J Cathey

R2: Digital Principles,3/e,Roger L

**ADDITIONAL BOOKS:**

A1**:** DigitalElectronics – A.P. Godse, U.A. Godse

A2**:** Analog and Digital principle.

**WEB REFERENCES:**

W1: nptel.ac.in/courses/106102062/16

W2: nptel.ac.in/courses/117105080/3

W3: nptel.ac.in/courses/117103064/21

W4: nptel.ac.in/courses/117106086/11

W5: <http://nptel.ac.in/courses/117105080/26>

W6: http://nptel.ac.in/courses/117105080/32

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